



# H55H-I V1.0A

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## REVISION HISTORY:

Rev	Date	Notes
A	2009/10/15	First release
1.0	2009/12/15	1. modify EC18 to small CAP 2. swap EC26 and EC27, change EC26 to lower CAP 3. modify H_VTTPWRGD 4. remove C36, C40 5. add LPC_DEBUG header 6. keep SPI ROM far away L8 7. SPI_DEBUG signal add damping 8. change Memory DIMM2 SMB address 9. add VAXG switching MOS damping 10. V_3P3_DAC_FB add 10U CAP 11. add CPU SKTOCC 12. Super I/O pin14 remove 10U CAP, add 22n CAP(follow ITE)
1.0A	2010/01/19	1. SWAP SU11 pin3.4, fix front USB loss power in S3 state

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### IMPORTANT NOTES ABOUT THIS SCHEMATIC

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

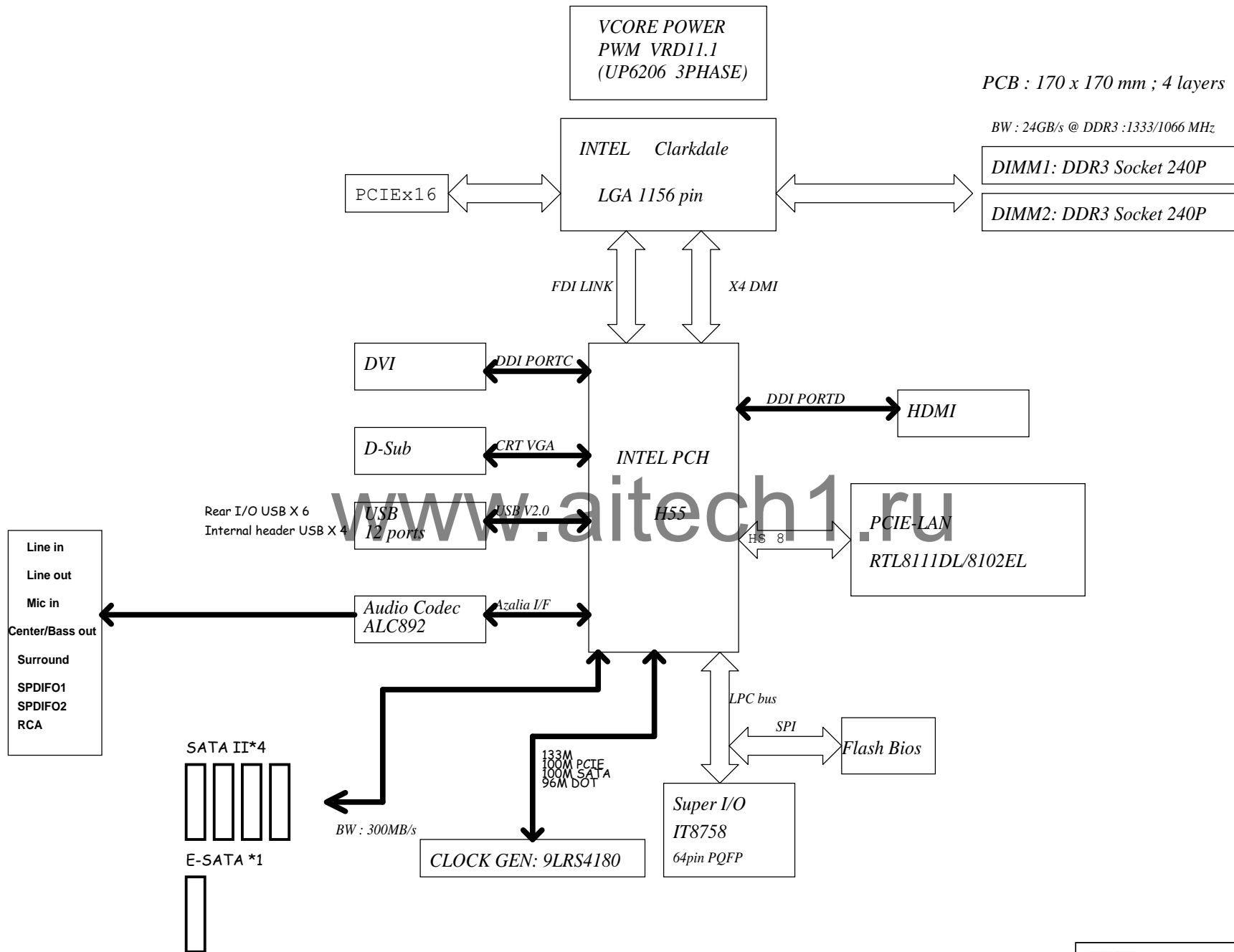
2) DESIGN NOTES in yellow are notes of caution.

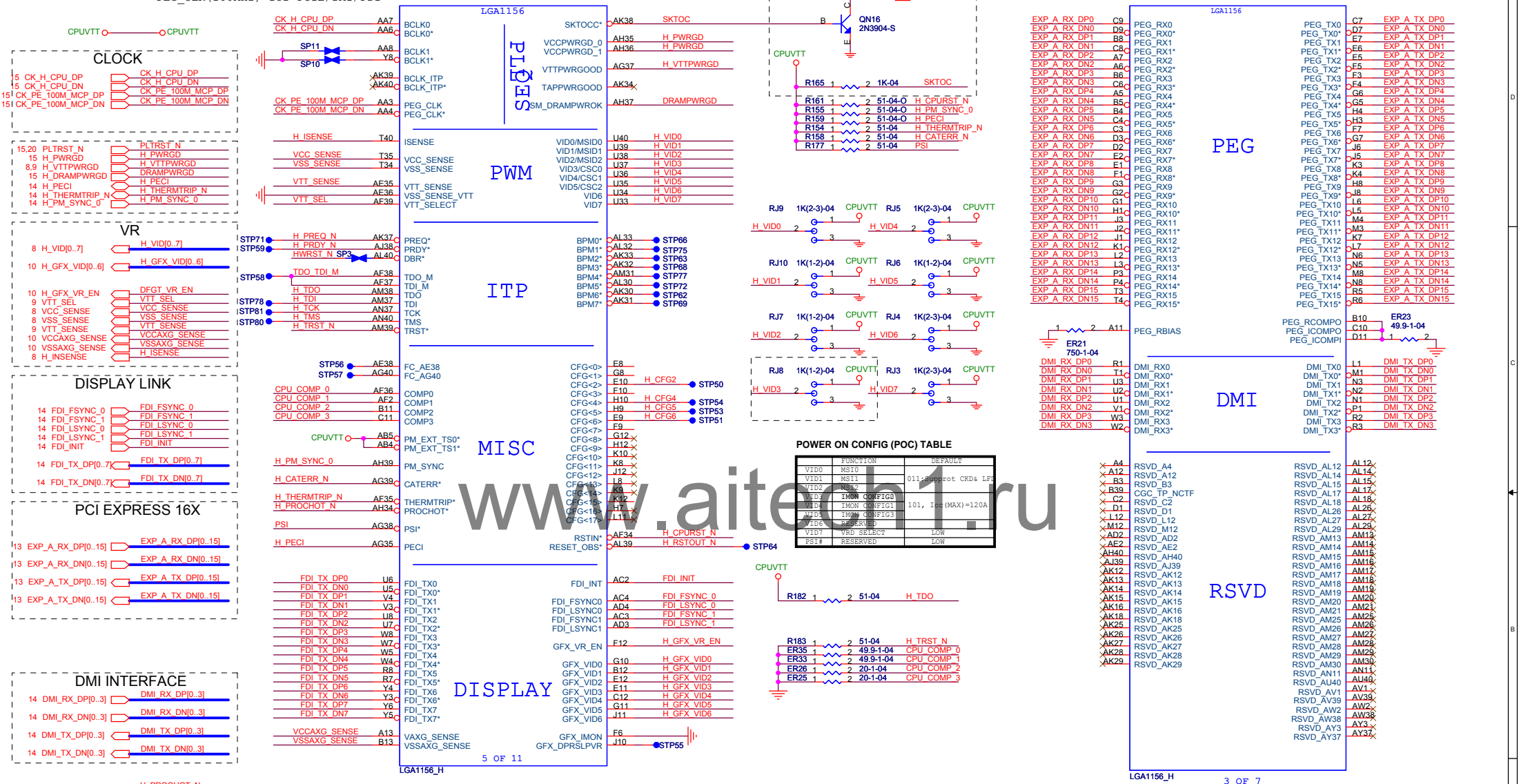


3) DESIGN NOTES in red are critical, and must be understood and followed.

PCB STACK: L1:TOP  
L2:POWER  
L3:IN1  
L4:IN2  
L5:GND  
L6:BOTTOM

Elitegroup Computer Systems		
Title: Cover Page		
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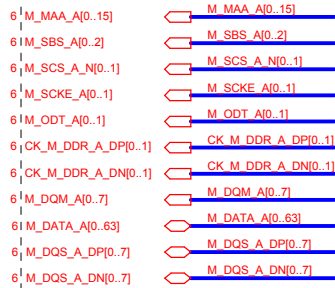


VIDD	FUNCTION	DEFAULT
VIDD0	MS10	
VIDD1	MS11	011:Support CKD6 L
VIDD2	MS12	
VIDD3	IMON CONFIG0	
VIDD4	IMON CONFIG1	101, 1cc (MAX)=120A
VIDD5	IMON CONFIG3	
VIDD6	RESERVED	
VIDD7	VRD SELECT	LOW
PS1#	RESERVED	LOW

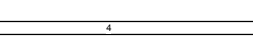
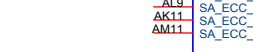
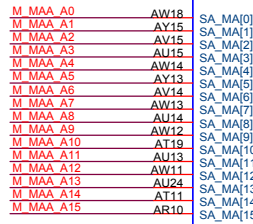
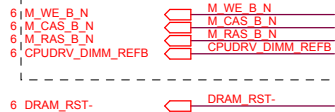
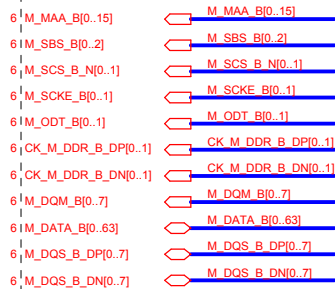
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8

CFG	H	L	DESCRIPTION
0	RSVD		PEG SEL0
1	RSVD		PEG SEL1
2	RSVD		PEG SEL2
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLE	ENABLE	DP PRESENCE
5	RSVD		
6	RSVD		
7	RSVD		ENGINEERING EXPERIMENT
15	RSVD		ENGINEERING EXPERIMENT

# CHANNEL A



# CHANNEL B



CPUA

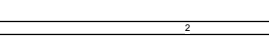
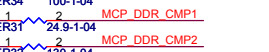
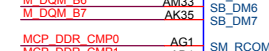
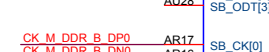
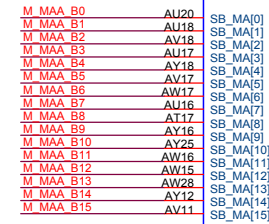
LGA1156

LGA1156\_H

1 OF 7

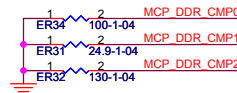
CPUB

LGA1156



DDR\_B

2 OF 7

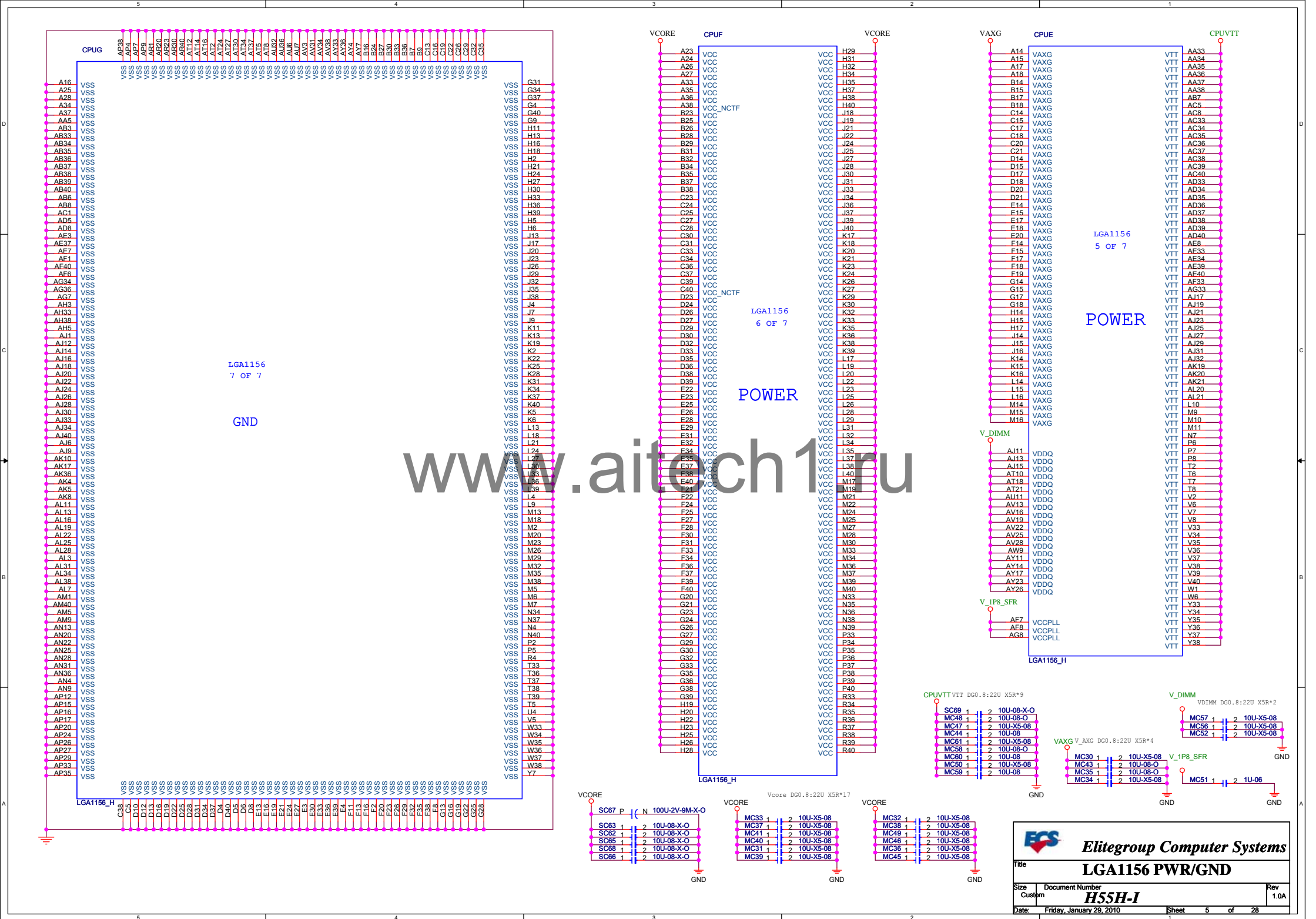


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Title **LGA1156 DDR3 MEMORY**

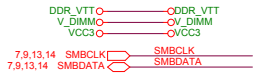
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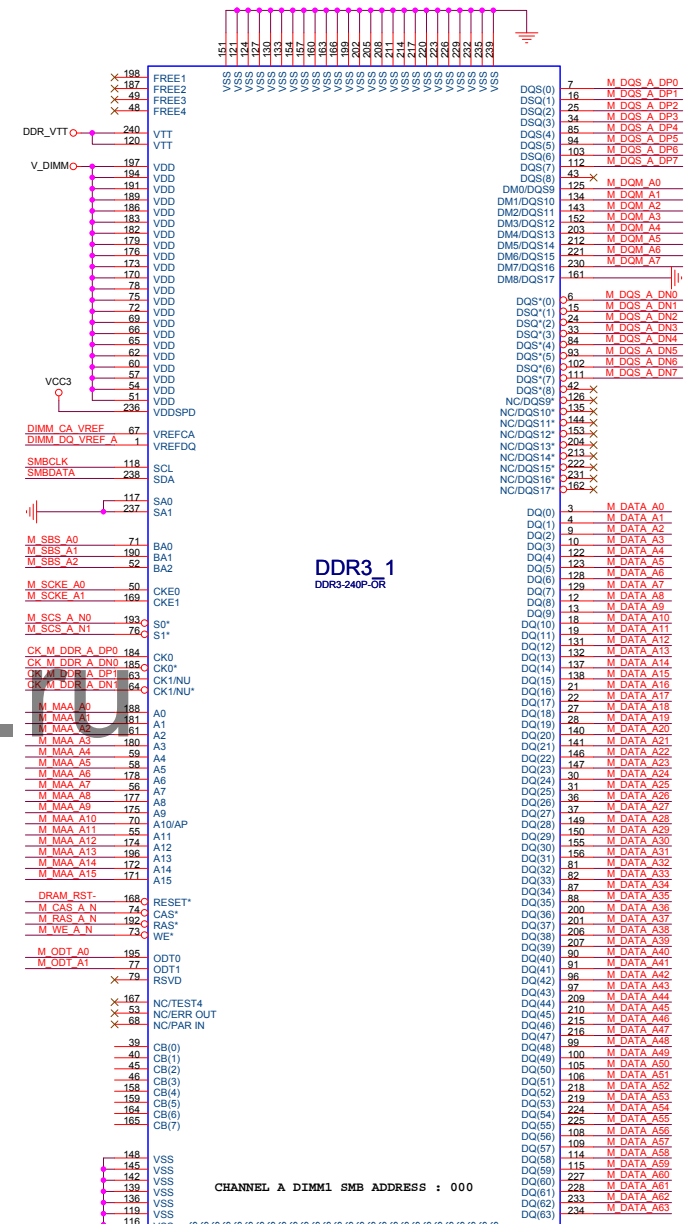
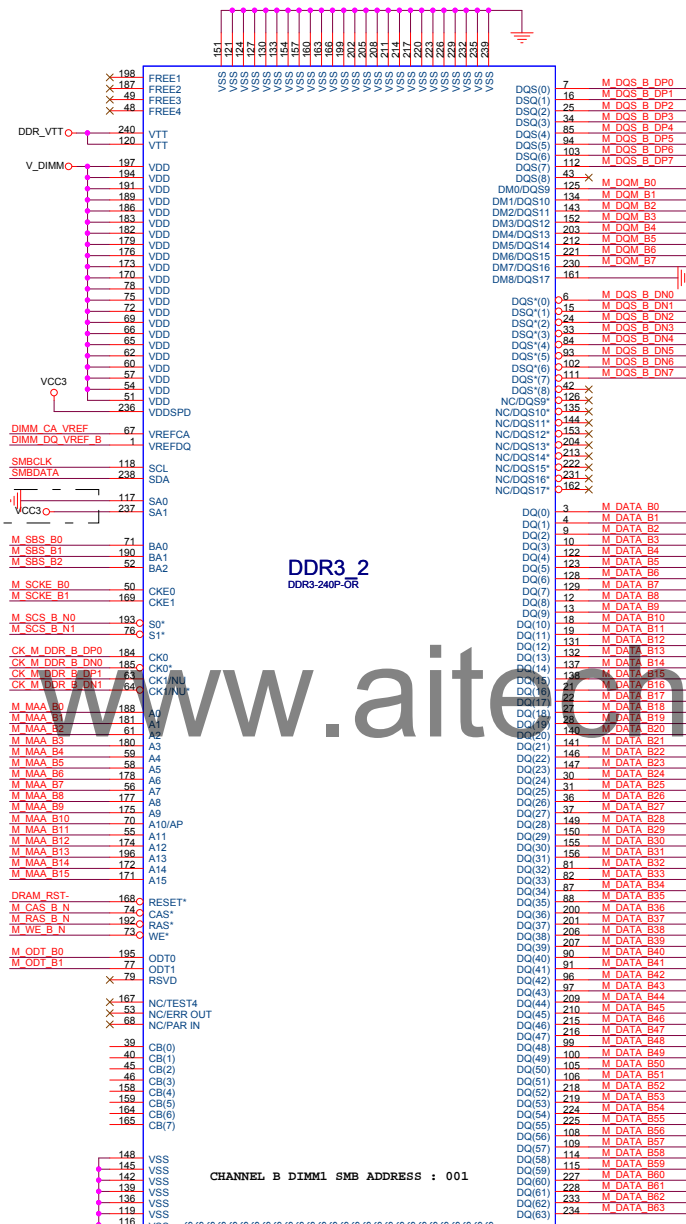
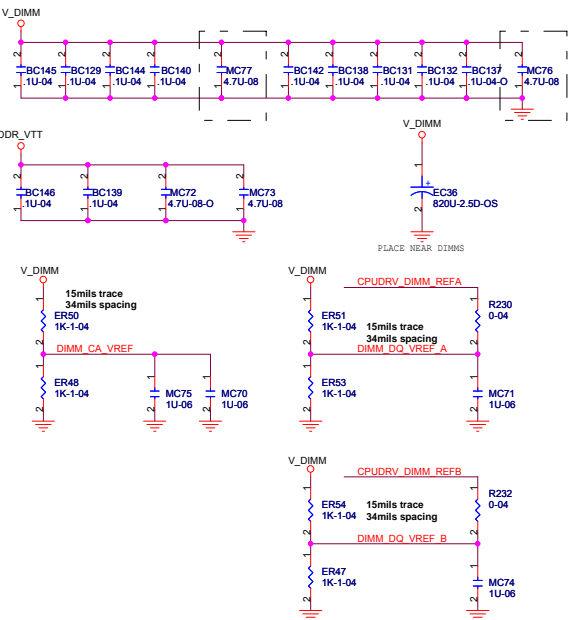
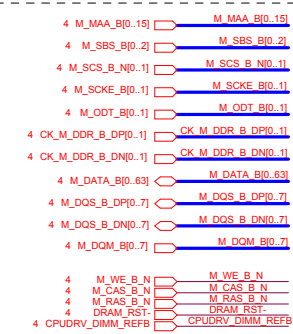
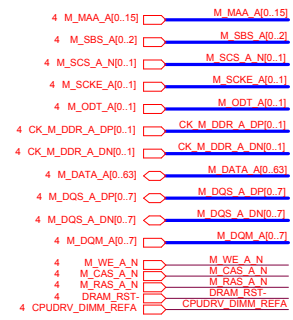
## External Connection



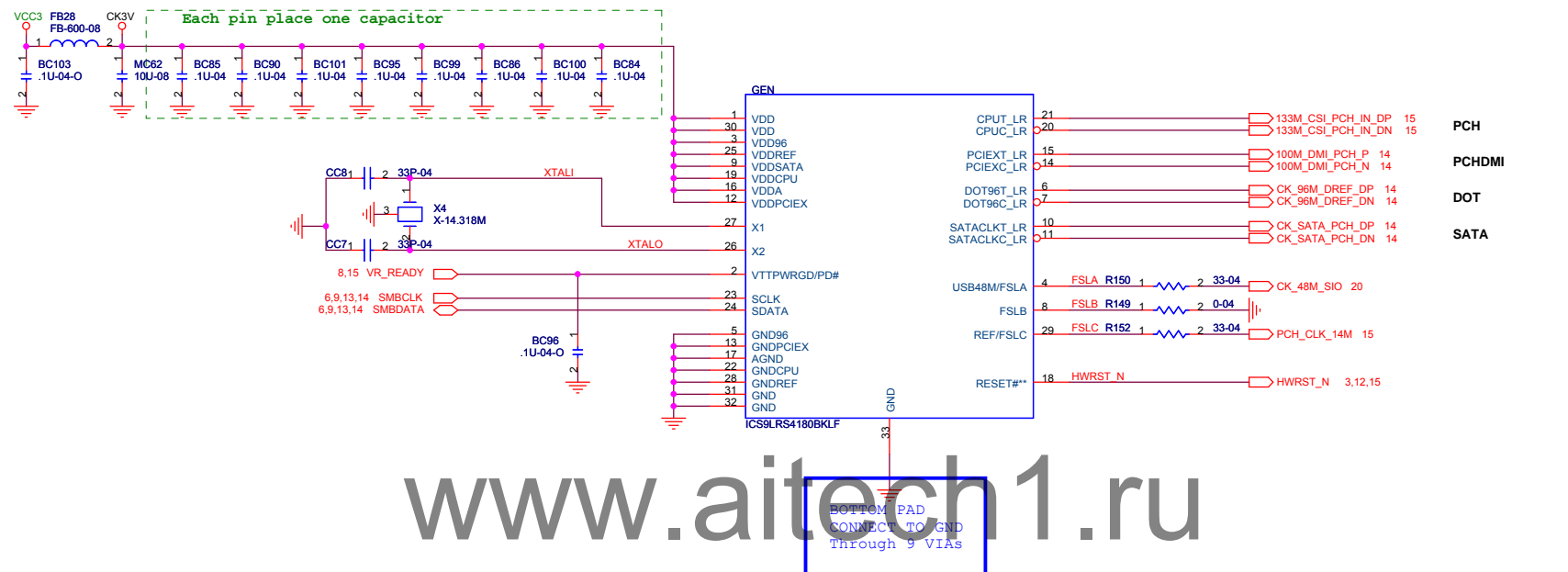
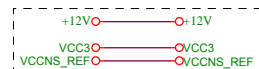
COMMON

ChannelA

ChannelB

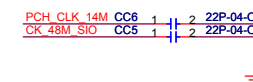


## External Connection

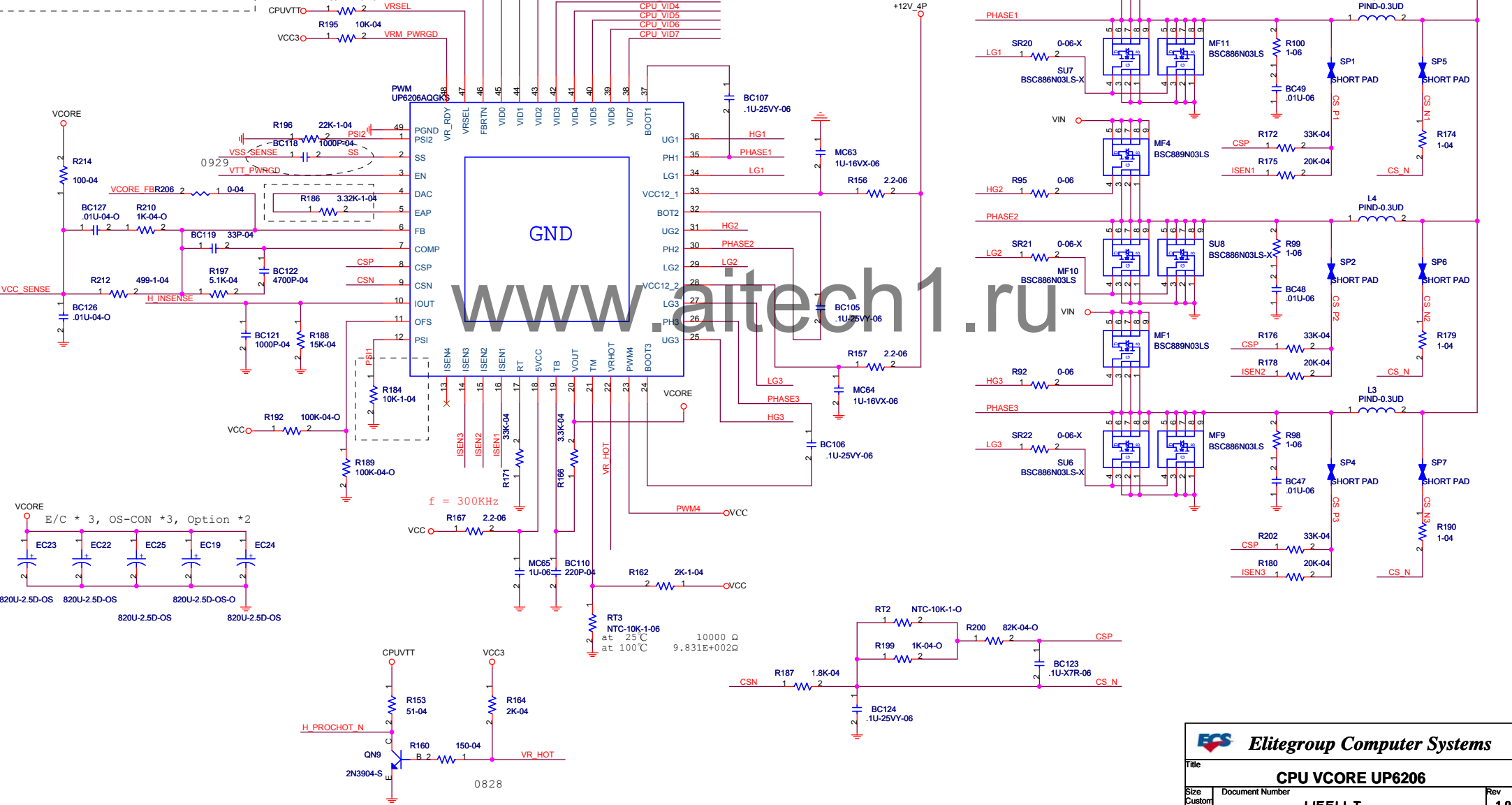
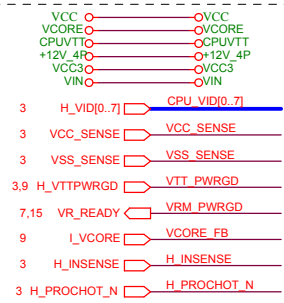


FSLC,FSLB,FSLA = 001, CPU\_CLK = 133MHz

FSLC (B0b2)	FSLB (B0b1)	FSLA (B0b0)	CPU MHz	PCIE MHz	SATA MHz	DOT96 MHz
0	0	1	133.33	100	100	96.00
1	0	1	100.00	100	100	96.00



# External Connection

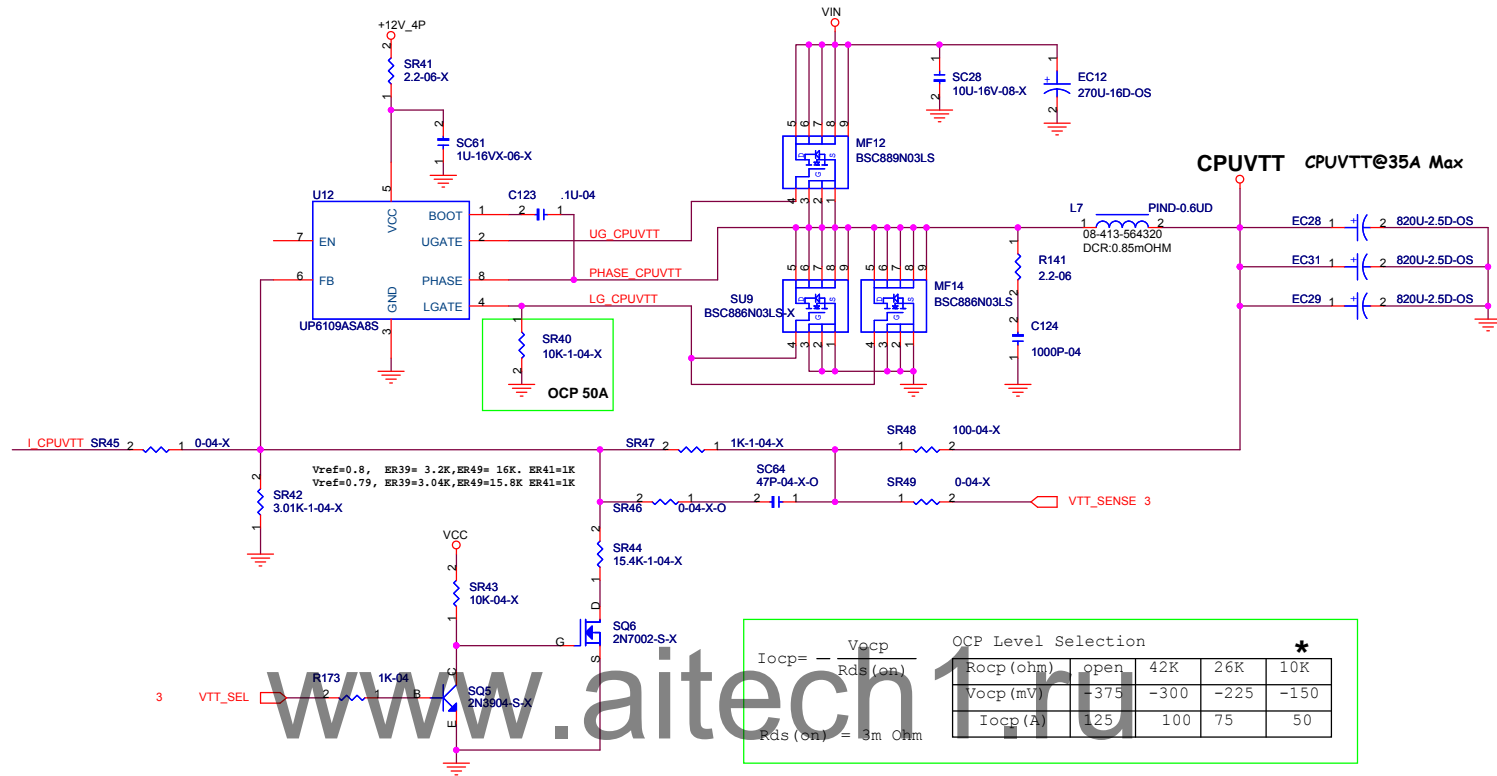




## External Connection



VTT_SEL	CPUVTT
1	1.05V
0	1.10V



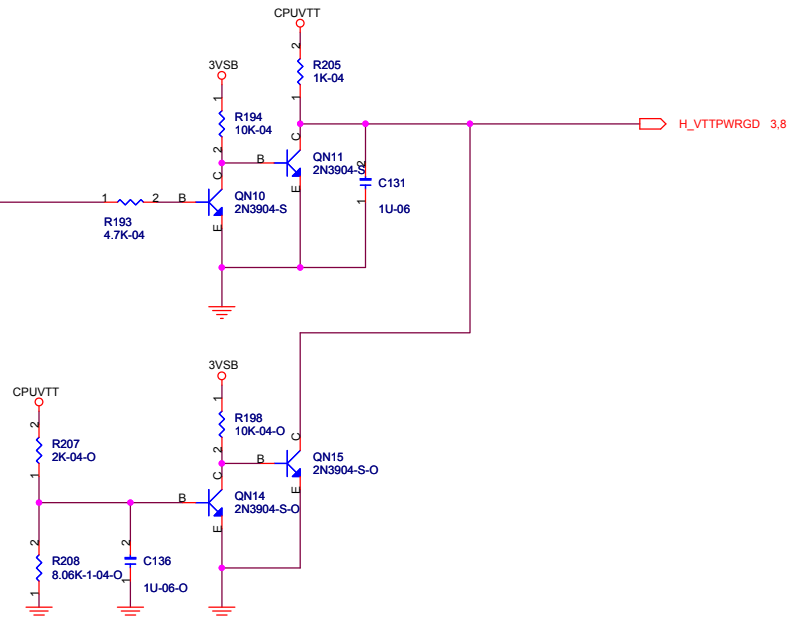
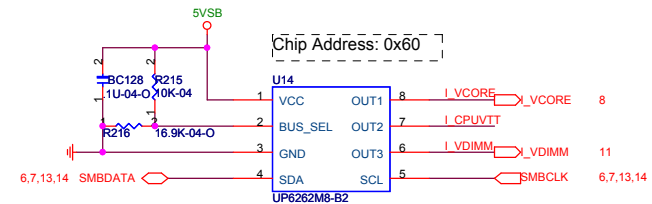
$$I_{ocp} = - \frac{V_{ocp}}{R_{ds(on)}}$$

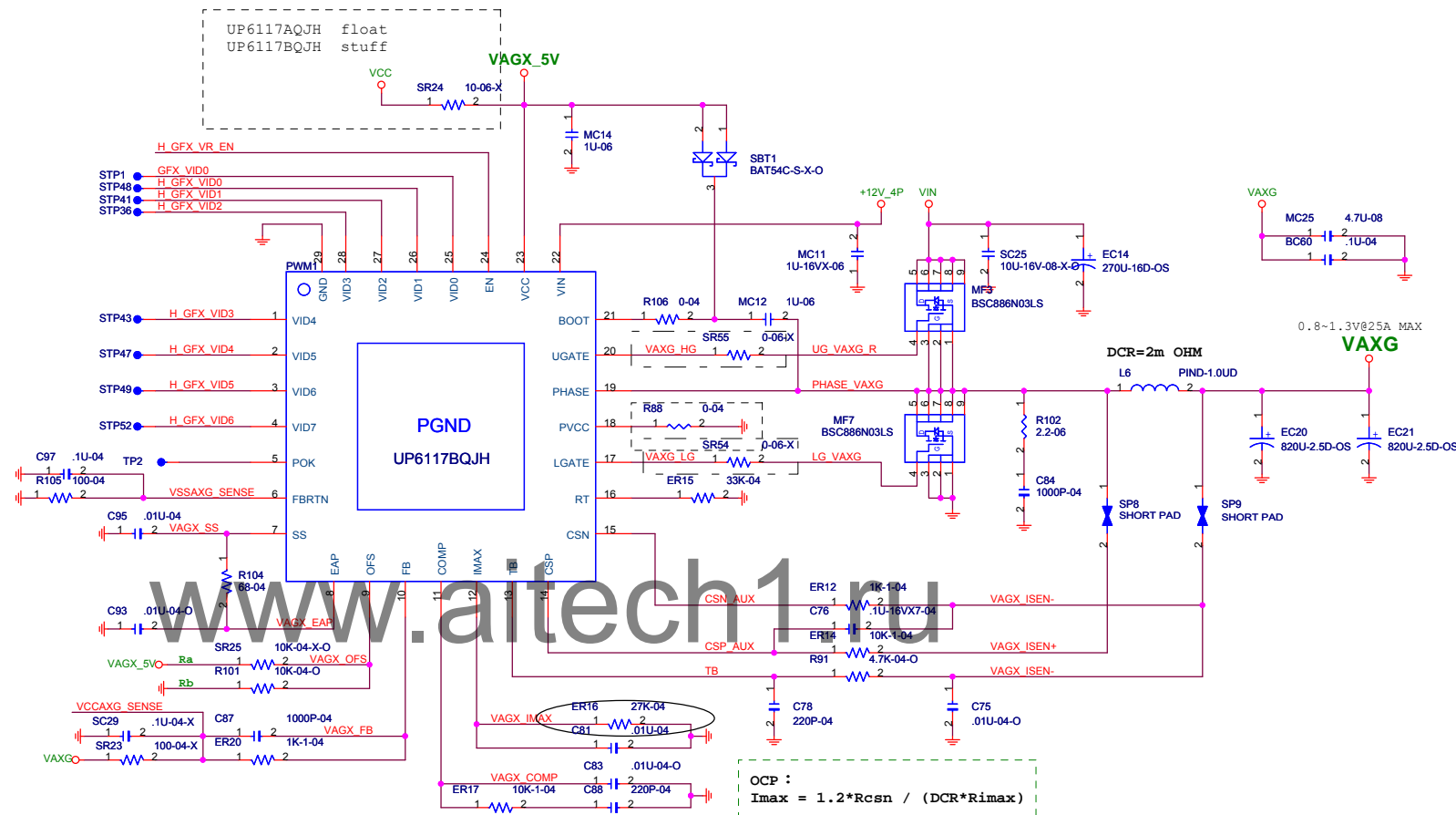
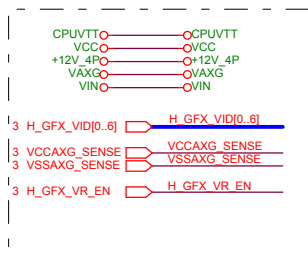
$R_{ds(on)} = 3m\ \Omega$

OCF Level Selection \*

	Rocp (ohm)	open	42K	26K	10K
Vocp (mV)	-375	-300	-225	-150	
Iocp (A)	125	100	75	50	

uP6262的電流輸出與ΔVout的關係如下：  
選取從uP6262輸出的方向為正，則VCORECPUVTT的ΔVout為：  
ΔVout = -Ic \* RFB;  
RFB為：  
1. For VCORE, RFB = Rvcore = 499 OHM;  
2. For CPUVTT, RFB = Rb = 1K;  
3. For VDIMM, RFB = Rvdim = 1K

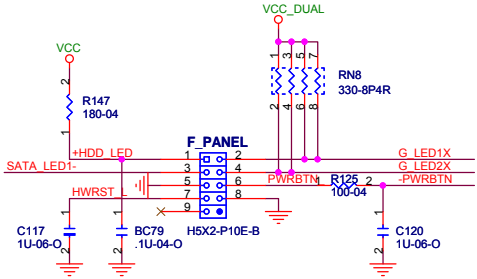
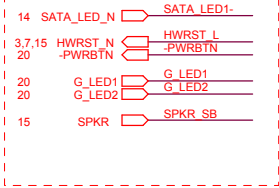




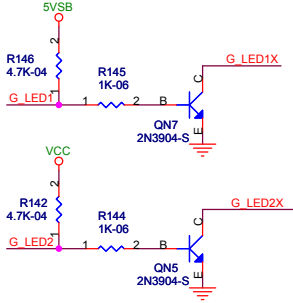
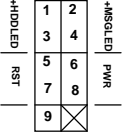


FRONT PANEL

External Connection



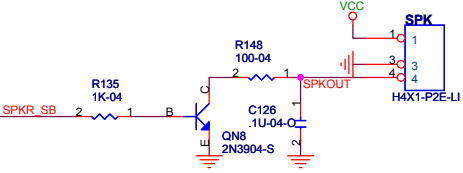
F. PANEL



	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	GB	YB	OFF	OFF

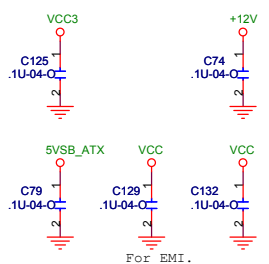
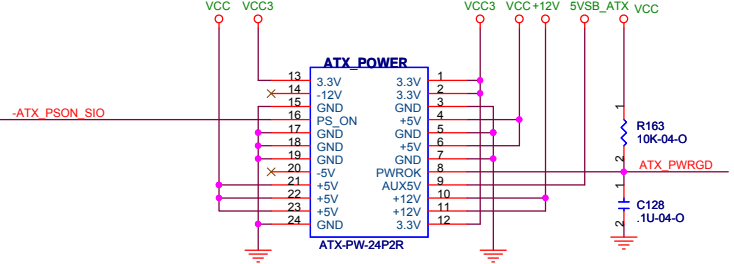
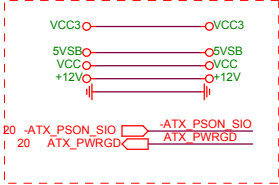
B: Blinking

BUZZER SPK Colay



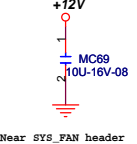
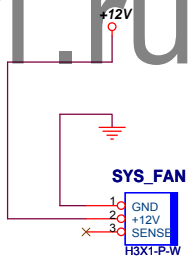
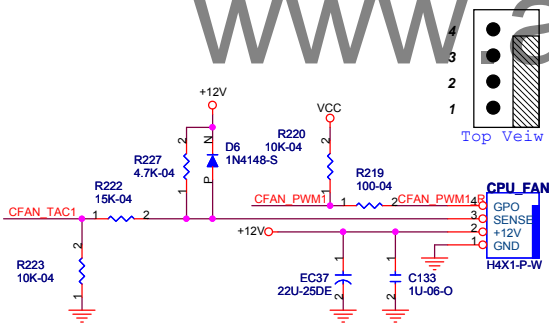
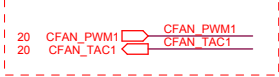
POWER CONNECTOR

External Connection

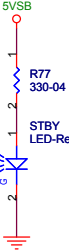
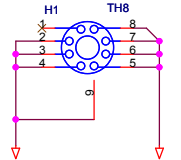
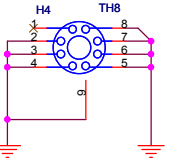
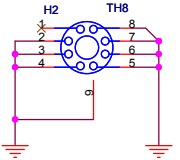
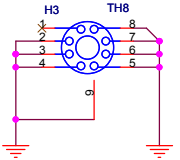


FAN

External Connection



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Title: **Front Panel,FAN,PowerConn**

Size: Custom

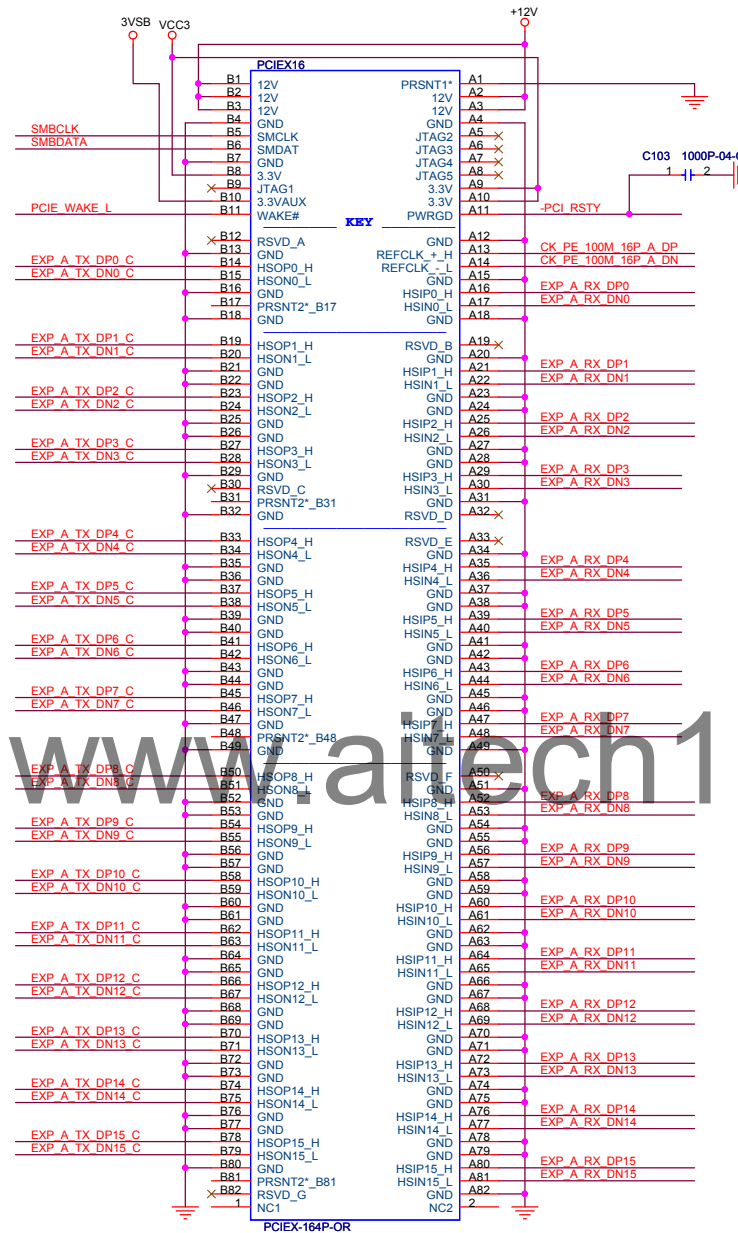
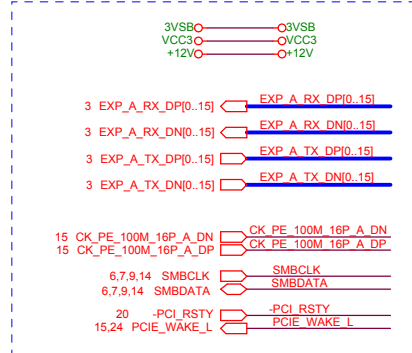
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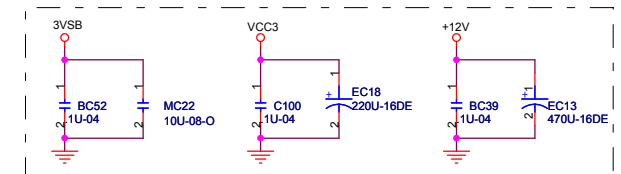
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## PCIEX16 External Connection



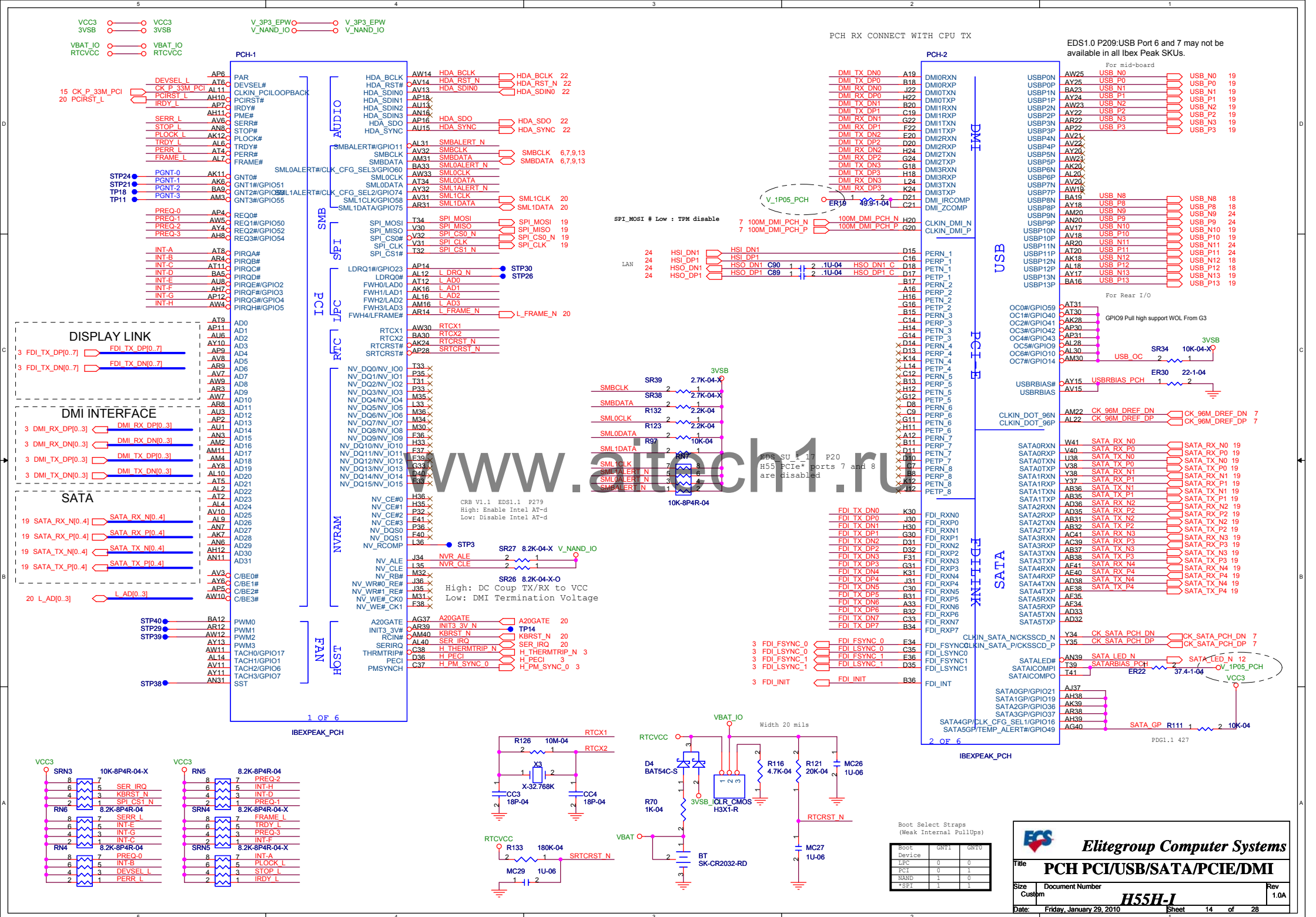
EXP A TX DP0 C	BC56	1	2	.1U-04	EXP A TX DP0
EXP A TX DN0 C	BC57	1	2	.1U-04	EXP A TX DN0
EXP A TX DP1 C	BC58	1	2	.1U-04	EXP A TX DP1
EXP A TX DN1 C	BC59	1	2	.1U-04	EXP A TX DN1
EXP A TX DP2 C	BC61	1	2	.1U-04	EXP A TX DP2
EXP A TX DN2 C	BC62	1	2	.1U-04	EXP A TX DN2
EXP A TX DP3 C	BC64	1	2	.1U-04	EXP A TX DP3
EXP A TX DN3 C	BC63	1	2	.1U-04	EXP A TX DN3
EXP A TX DP4 C	BC65	1	2	.1U-04	EXP A TX DP4
EXP A TX DN4 C	BC67	1	2	.1U-04	EXP A TX DN4
EXP A TX DP5 C	BC69	1	2	.1U-04	EXP A TX DP5
EXP A TX DN5 C	BC71	1	2	.1U-04	EXP A TX DN5
EXP A TX DP6 C	BC73	1	2	.1U-04	EXP A TX DP6
EXP A TX DN6 C	BC75	1	2	.1U-04	EXP A TX DN6
EXP A TX DP7 C	BC76	1	2	.1U-04	EXP A TX DP7
EXP A TX DN7 C	BC78	1	2	.1U-04	EXP A TX DN7
EXP A TX DP8 C	BC81	1	2	.1U-04	EXP A TX DP8
EXP A TX DN8 C	BC80	1	2	.1U-04	EXP A TX DN8
EXP A TX DP9 C	BC82	1	2	.1U-04	EXP A TX DP9
EXP A TX DN9 C	BC83	1	2	.1U-04	EXP A TX DN9
EXP A TX DP10 C	BC87	1	2	.1U-04	EXP A TX DP10
EXP A TX DN10 C	BC91	1	2	.1U-04	EXP A TX DN10
EXP A TX DP11 C	BC92	1	2	.1U-04	EXP A TX DP11
EXP A TX DN11 C	BC97	1	2	.1U-04	EXP A TX DN11
EXP A TX DP12 C	BC102	1	2	.1U-04	EXP A TX DP12
EXP A TX DN12 C	BC104	1	2	.1U-04	EXP A TX DN12
EXP A TX DP13 C	BC108	1	2	.1U-04	EXP A TX DP13
EXP A TX DN13 C	BC109	1	2	.1U-04	EXP A TX DN13
EXP A TX DP14 C	BC111	1	2	.1U-04	EXP A TX DP14
EXP A TX DN14 C	BC112	1	2	.1U-04	EXP A TX DN14
EXP A TX DP15 C	BC116	1	2	.1U-04	EXP A TX DP15
EXP A TX DN15 C	BC114	1	2	.1U-04	EXP A TX DN15

Please place the caps close to PCI-EX16 Slot.

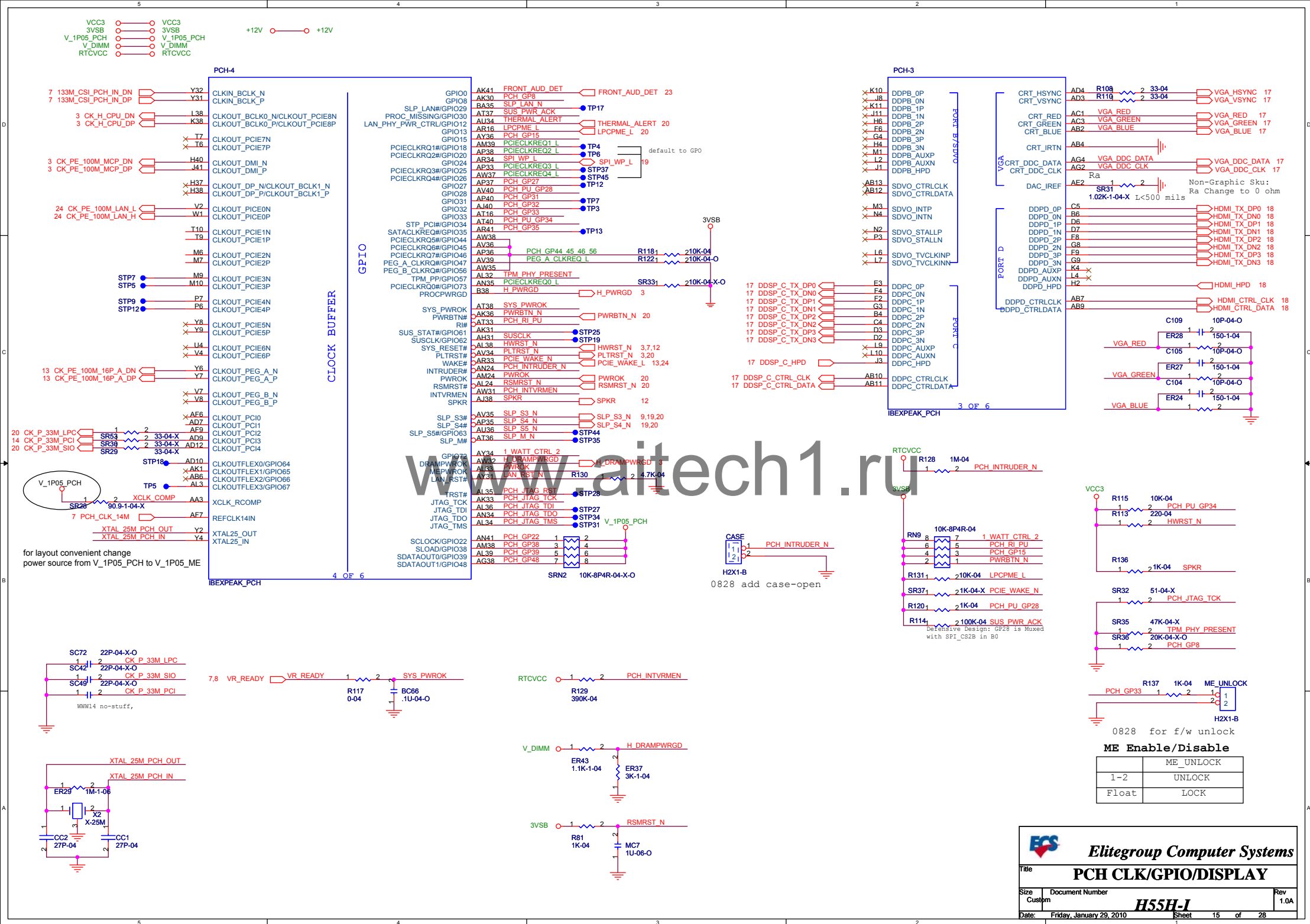


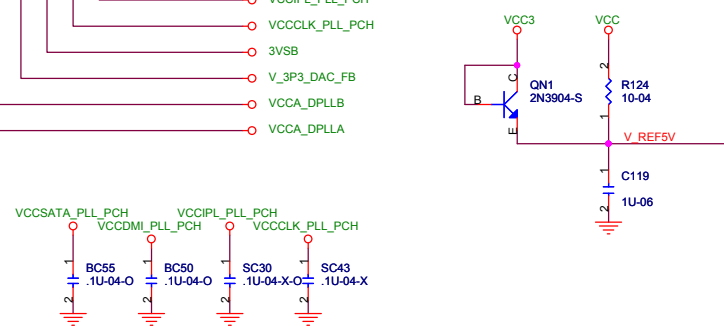
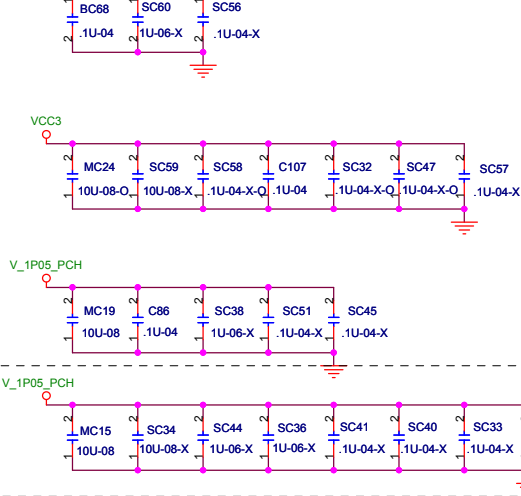
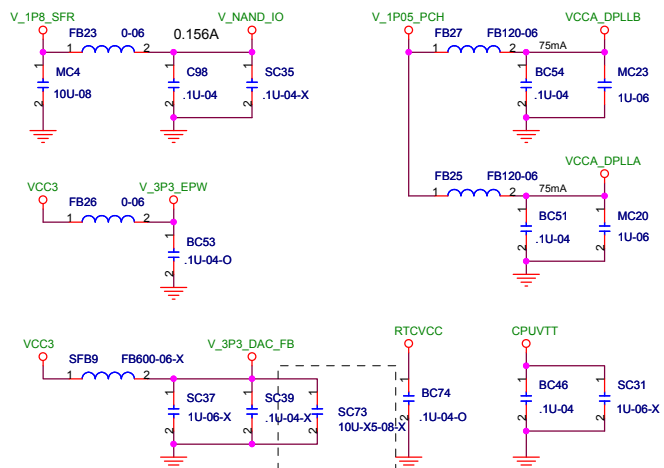
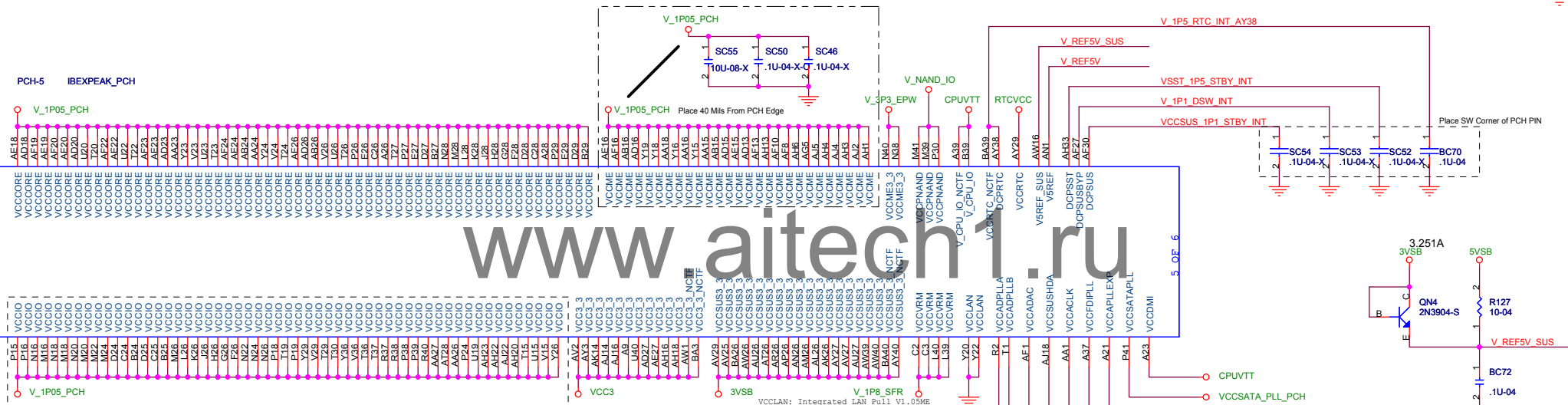
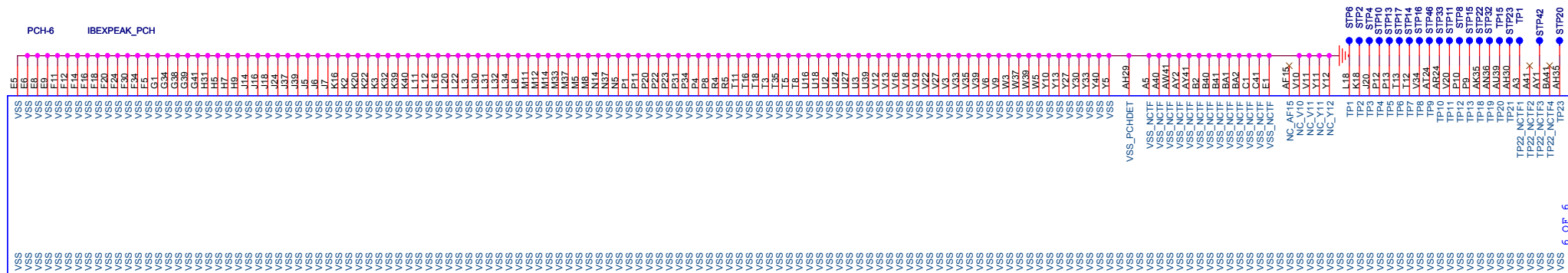
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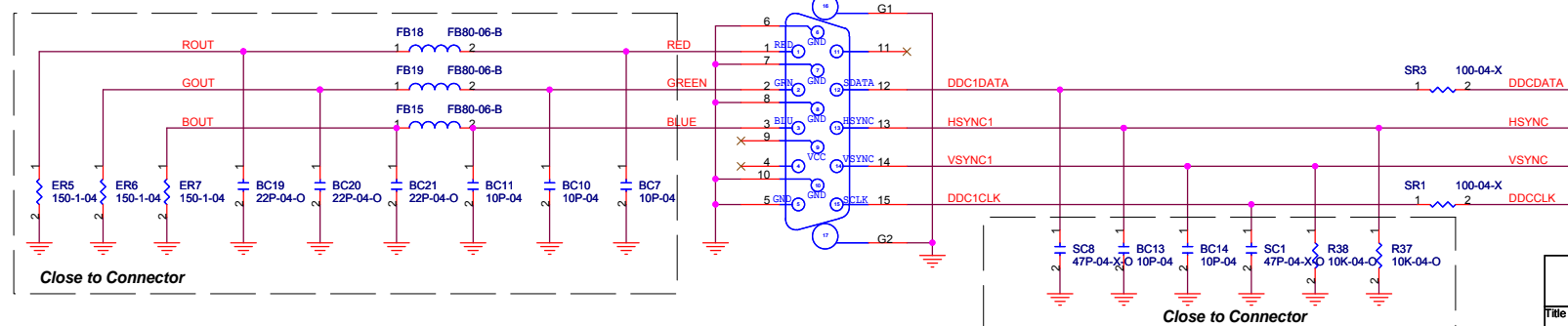
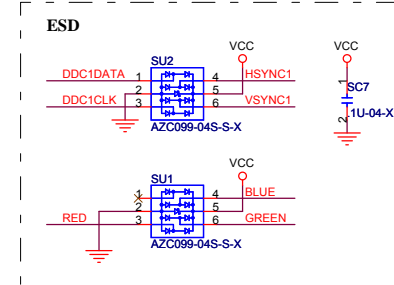
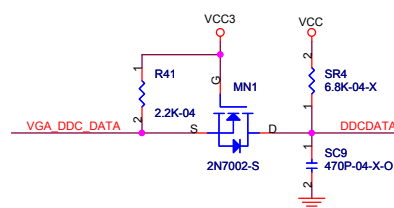
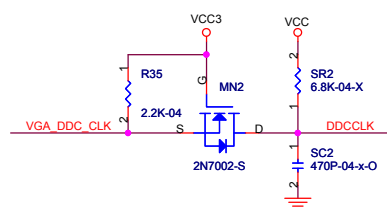
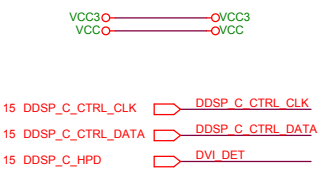
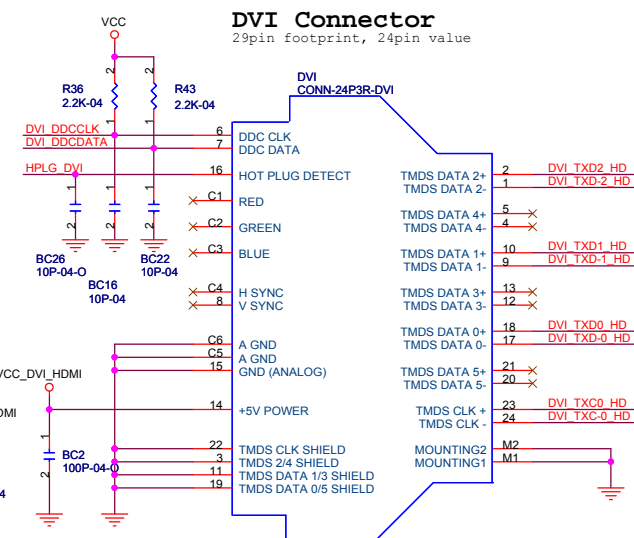
Title	PCIEX16 slot		
Size	Document Number	H55H-I	
Customer		Rev	1.0A
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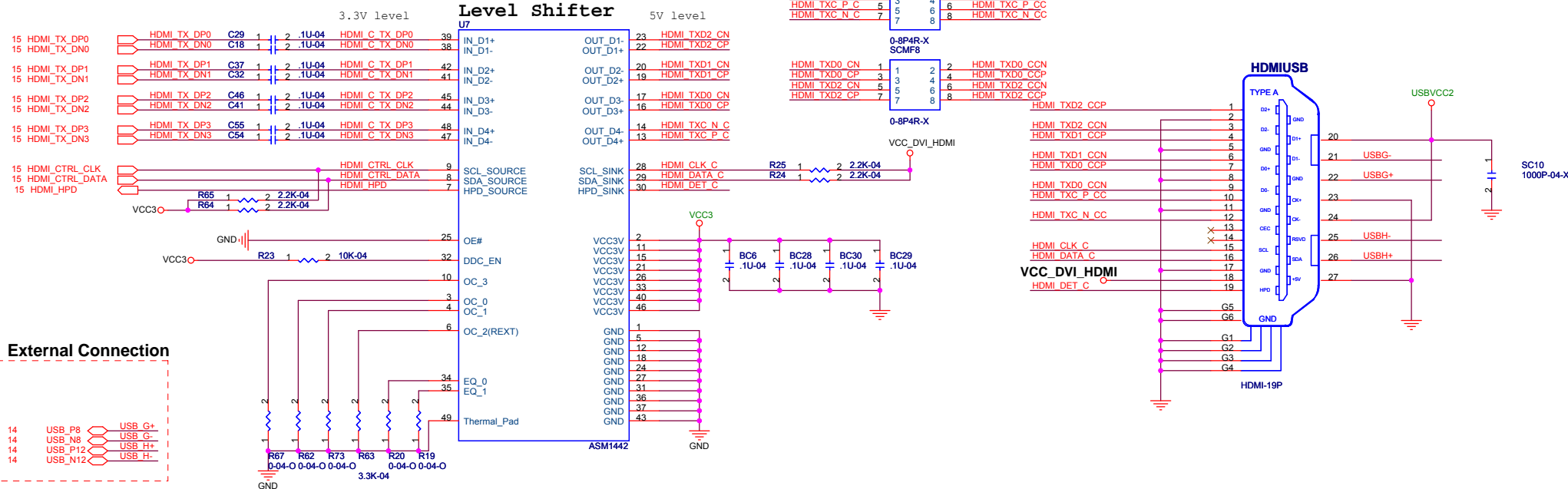




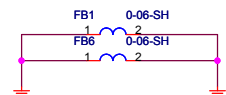
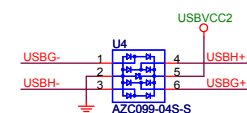
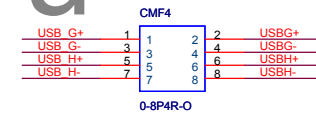




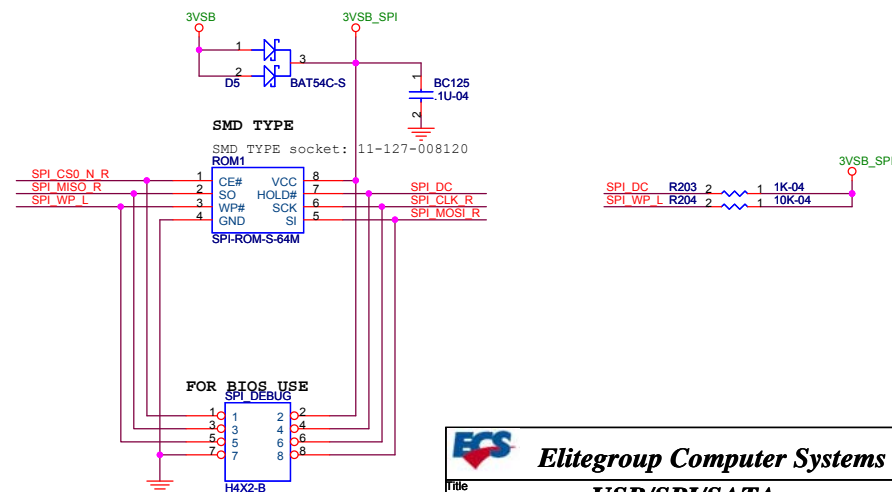
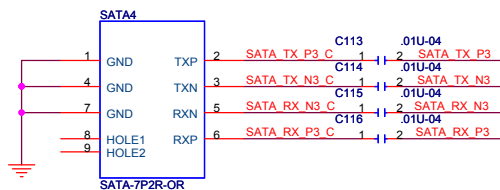
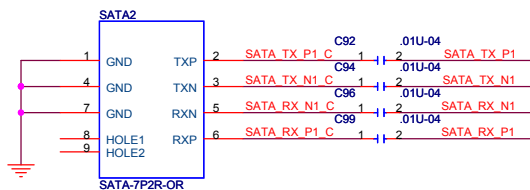
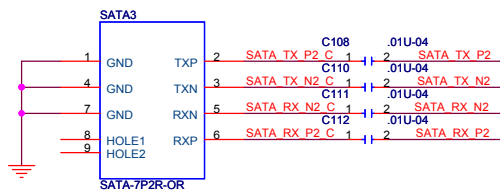
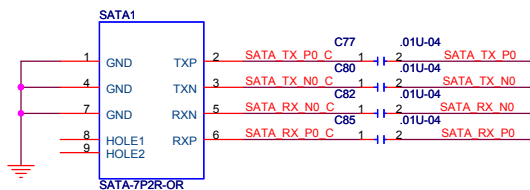
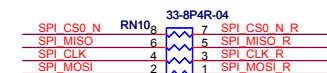
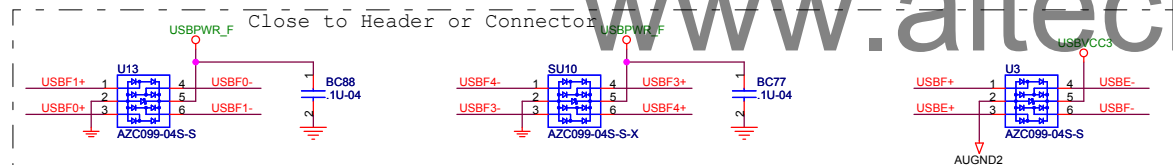
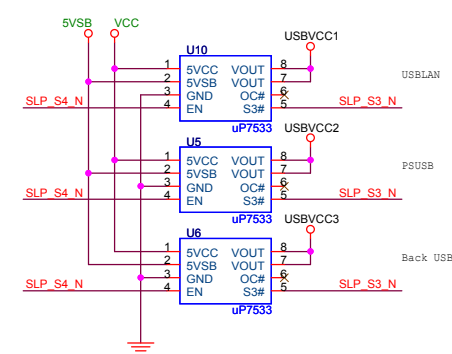
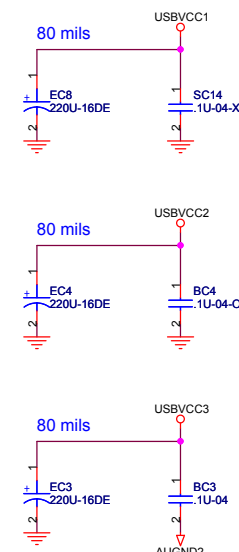
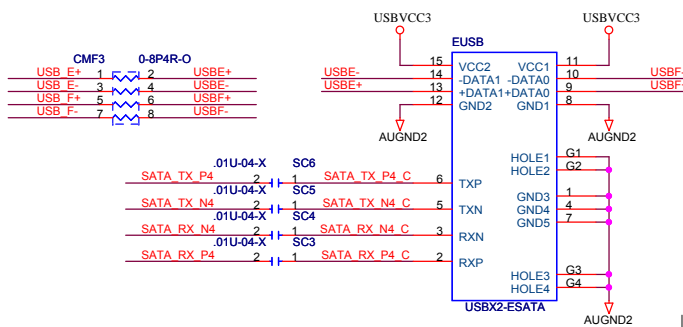
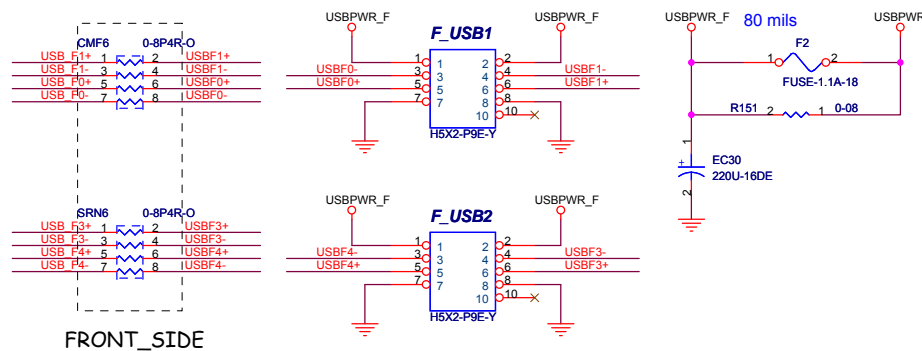
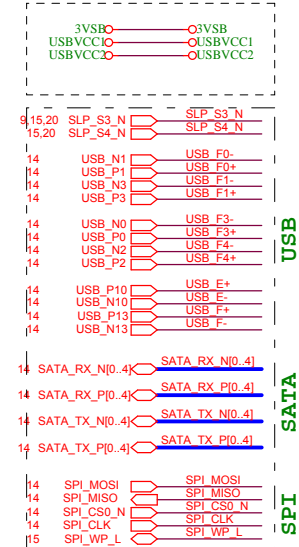
## HDMI+USB



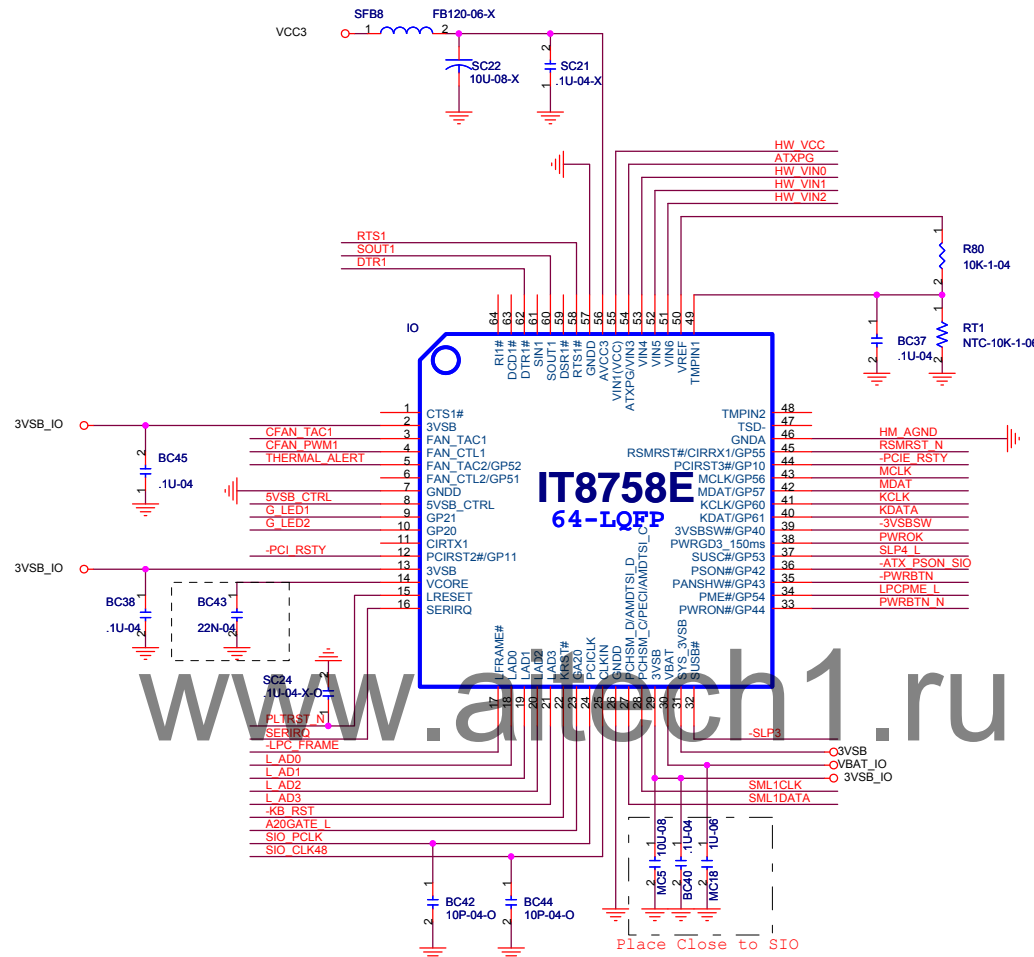
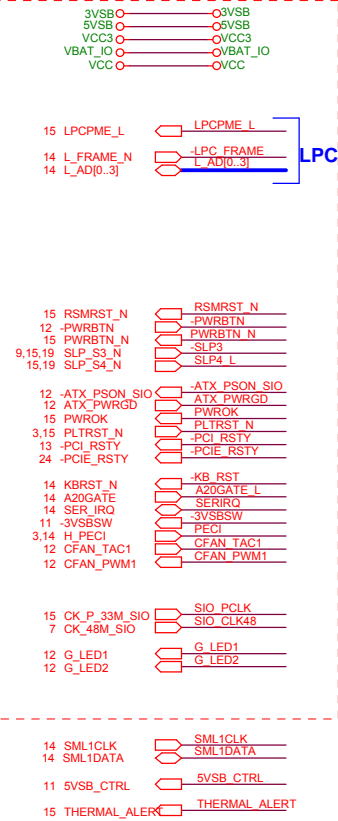
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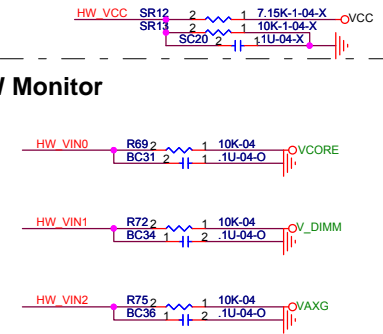
## External Connection



## External Connection

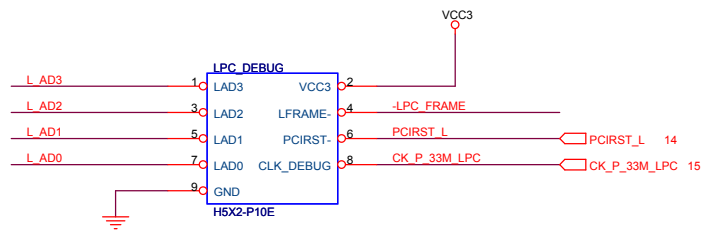
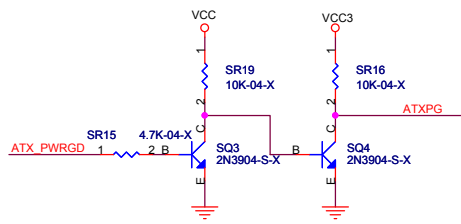
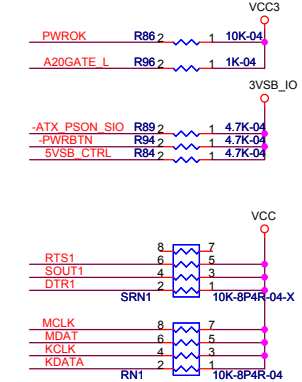


## H/W Monitor



## LPC Pull-ups

Note:  
Most pull-ups are provided





1080 : trace width 4 mil 50 ohm  
Trace Length 3150 mils  
Spacing: 1.clearance to itself 50/4/50(S:W:S)  
2.clearance to other signal 3W

ME\_UNLOCK(104)



JP-R

CLR\_CMOS(1-2)



JP-R

X3(WIRE)



JP-WI-P6.25

ROM1(104)

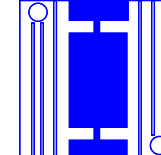


SPI-ROM-S-64M  
SMD 64M



CR2032

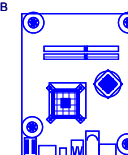
104 PCH1



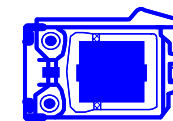
HEATSINK

Main Part:20-120-010991

PCB



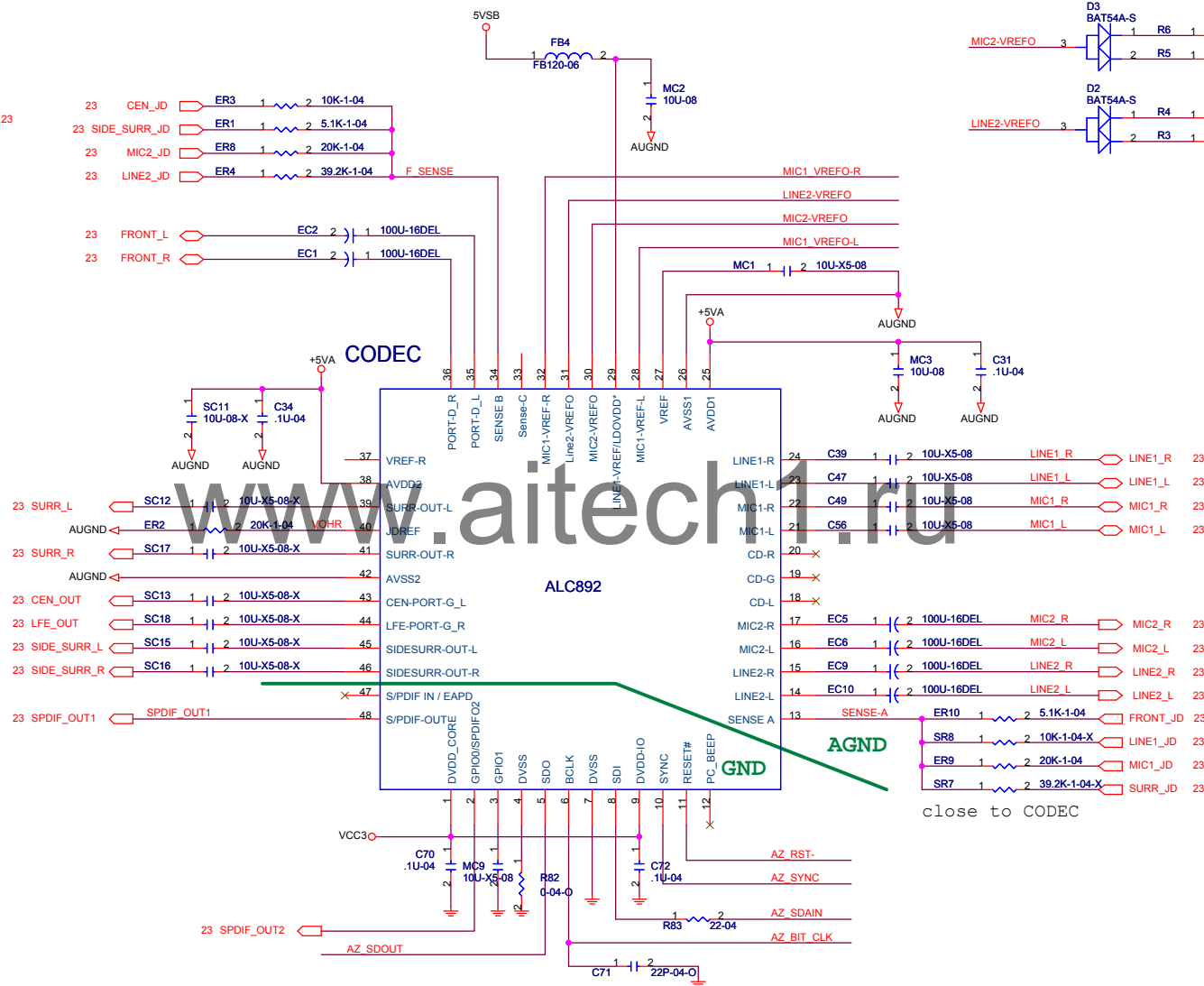
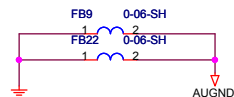
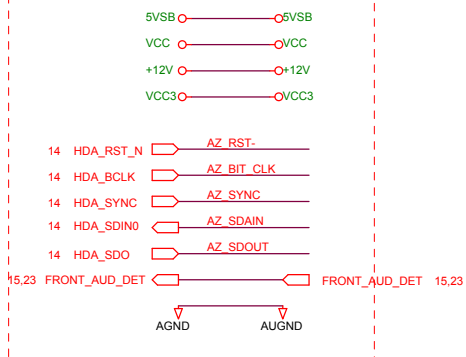
PCB-6layer



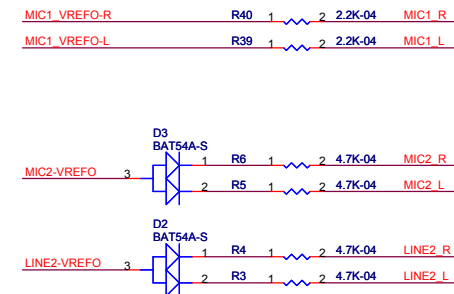
CPU(104)

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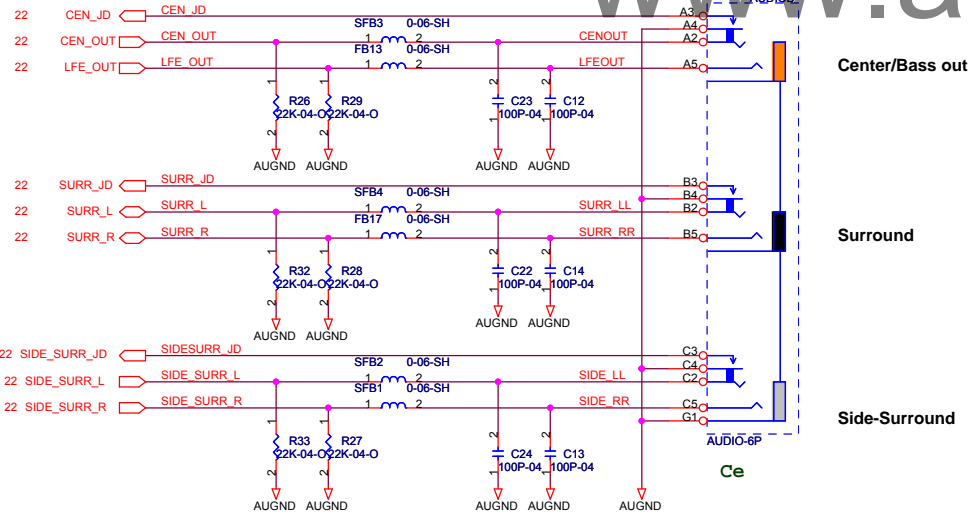
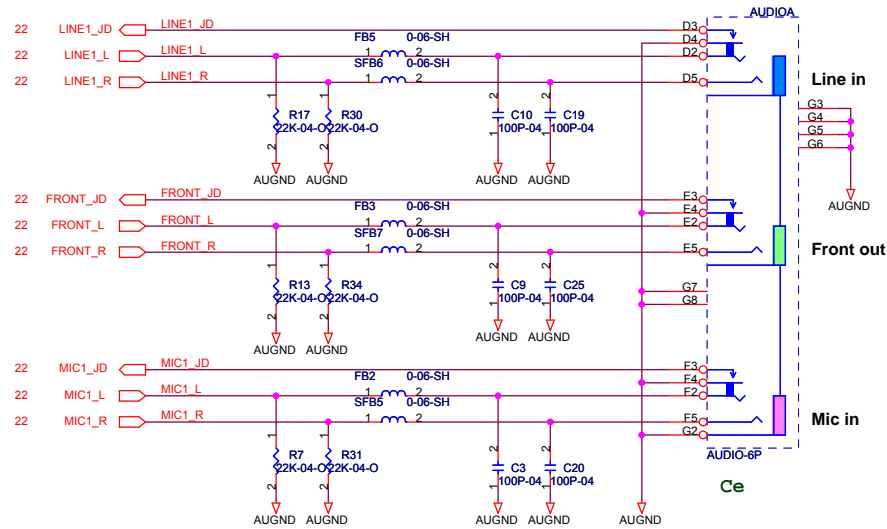
## External Connection



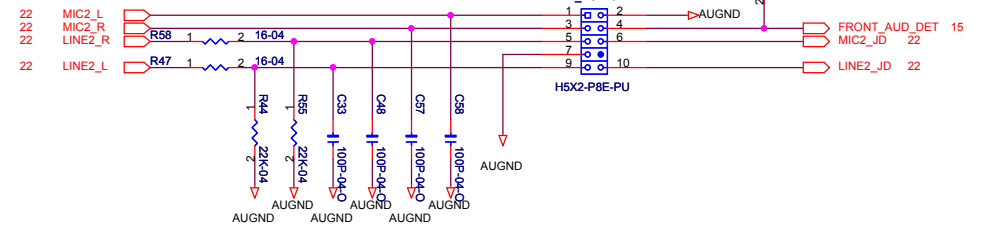
## Verfout bias for stereo microphone.



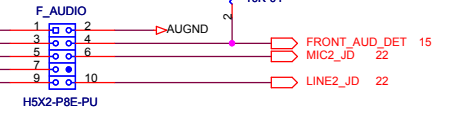
## Rear Panel Onboard Analog I/O



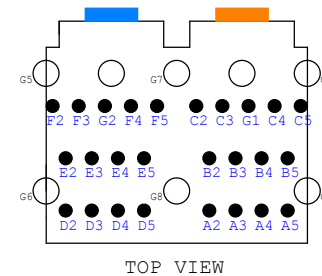
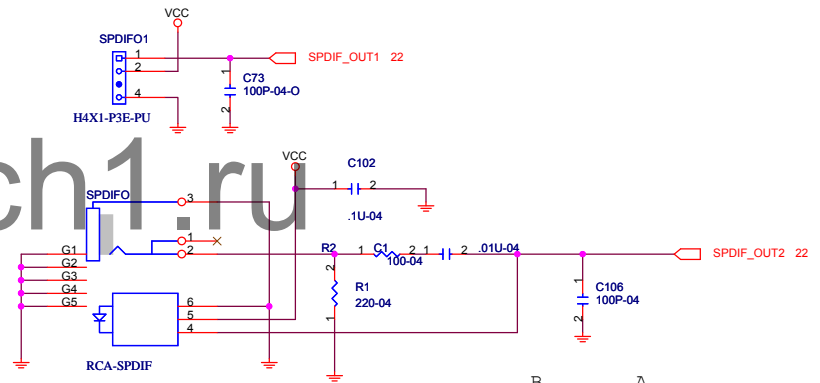
## FRONT-AUDIO



## HD



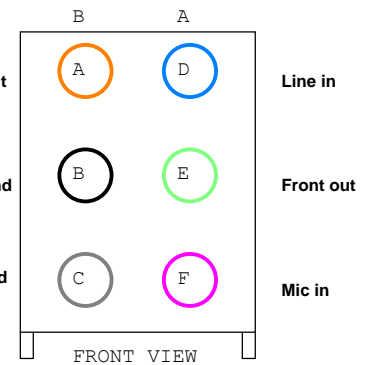
## SPDIF1-OUT



Center/Bass out

Back-Surround

Side-Surround



Line in

Front out

Mic in



ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P1
12V
+/-5%

SWITCH  
UP6206

SWITCH  
UP6117A

SWITCH  
UP6109

NPS08-S

VCC\_DUAL

RT9214-S SW  
POWER1.5V TO252 \* 2

OP324

7.789A

LDO 9173D

ADJ1086-S

LDO

LINEAR

NPS08-S

5V\_DUAL

(S0 , S1 , S3 , S4 , S5 )

USB X6 FR
VDD
5VDual
6.0A

USB X8 RL
VDD
5VDual
8.0A

2XPS
5VDual
1.0A

RTCVCC

BATTERY

SUPER I/O ITE8720		
5VSB	5V	15mA
VCC	5V	60mA
BAT 3.3V	3.3V	2uA
VCC3	3.3V	

Intel Havendale/Lynnfield CPU		
VCORE	VID 0.65~1.4	100A/110A
VAXG	VID 0.8~1.3	20A/25A
CPUVTT	1.1V	30/35A
VDDQ	1.5V	3/6A
VCC1_8	1.8V	1.1/1.35A

DDR3 2DIMMs		
V_DIMM	1.5V	7.2A
DDR_VTT	0.75V	0.83A

Intel PCH		
VCCDMI	1.1V	0.065A
V_CPU_IO	1.05/1.1V	<1mA
VCC_CORE	1.05V	1.629A
VCCIO	1.05V	3.251A
VCCLAN	1.05V	0.372A
VCCADPLLA	1.05V	0.075A
VCCADPLLB	1.05V	0.075A
VCCME	1.05V	2.222A
VCCACLK	1.05V	0.052A
VCCAPLLEXP	1.05V	0.045A
VCCFDIPLL	1.05V	0.037A
VCCSATAPLL	1.05V	0.031A
VCCVRM	1.8V	0.043A
VCCPNAND	1.8V	0.156A
VCCME3_3	3.3V	0.086A
VCCADAC	3.3V	0.069A
VCC3	3.3V	0.357A
VCCSUS3_3	3.3V	0.168A
VCCSUSHDA	3.3V	0.006A
RTCVCC	3.3V	0.002A

FANS		
V12s0	12V	200mA

CLK GEN		
VDD*	3.3V	10mA

DVI		
V3.3s0	3.3V	180mA

USB2.0		
V5Sdual	5V	0.5A*10

SPI		
VCC	5V	10mA

AZALIA		
DVDD	3.3V	0.3A
AVDD	5V	0.1A

LAN		
VDD33	3.3V	58mA
VDD12	5V	289mA

Internal VccVRM SWITCH

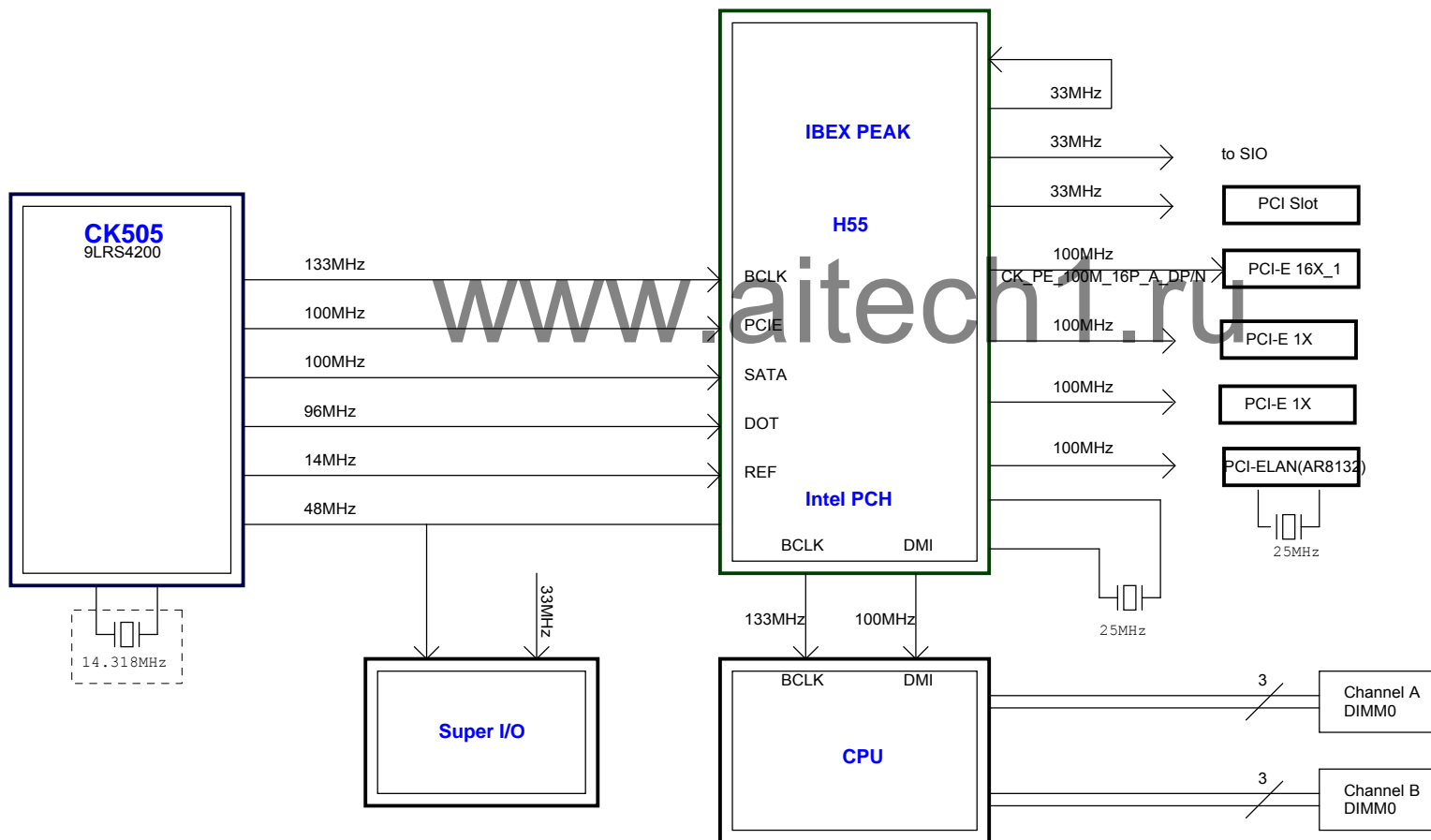
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**Elitegroup Computer Systems**

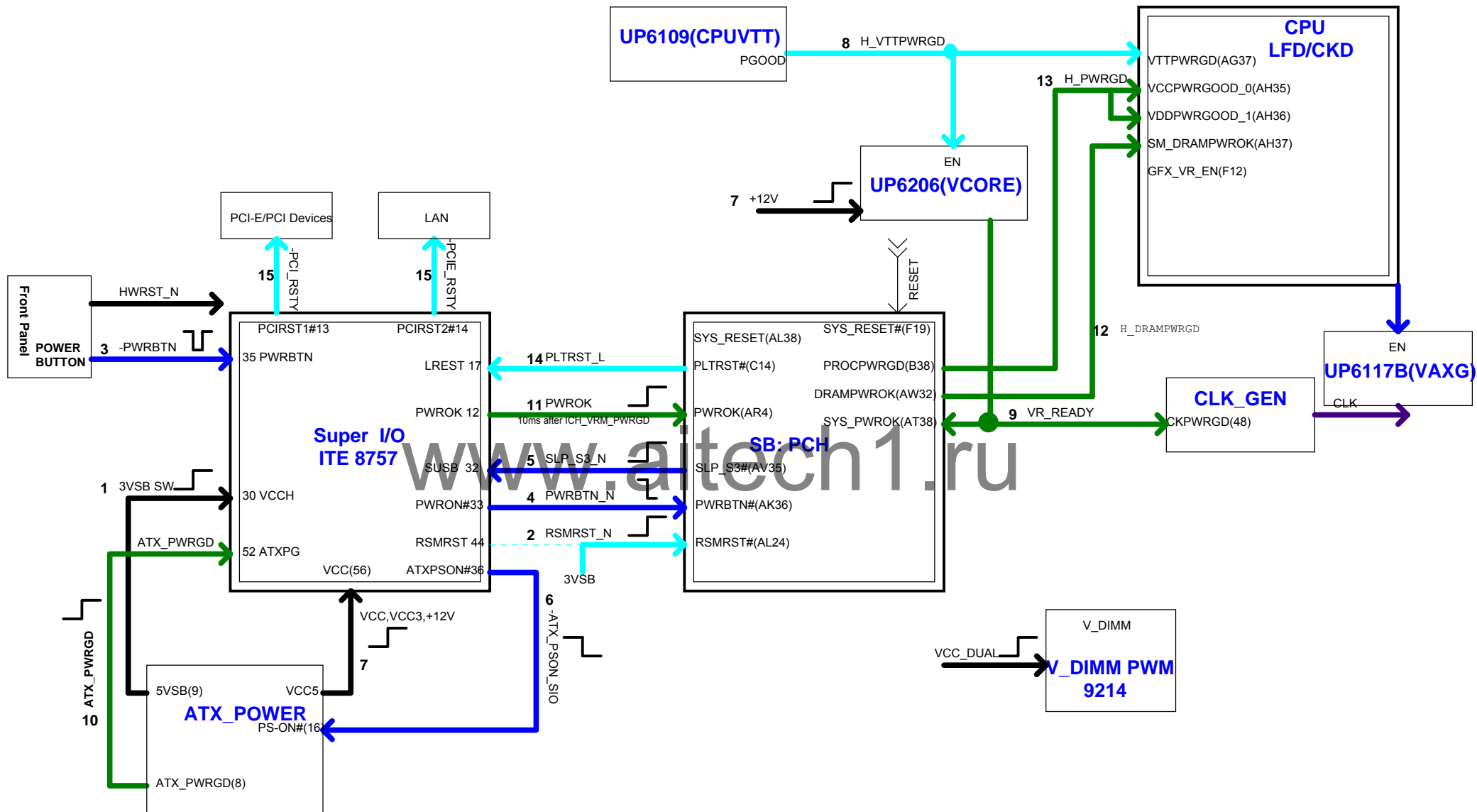
Title **Power Delivery Chart**

Size Custom Document Number **H55H-I** Rev **1.0A**

Date: Friday, January 29, 2010 Sheet 25 of 28







PCH STRAPS TABLE															
	H	L	DESCRIPTION	Default											
PGNT-3	(inter pu)	*Top Boot Block(-O)	A16 SWAP OVERRIDE Low: OVERRIDE	TestPoint											
PGNT-1, PGNT-0	<table border="1"><tr><td>BOOT_DEVICE</td><td>GNT0</td><td>GNT1</td></tr><tr><td>LPC</td><td>0</td><td>0</td></tr><tr><td>PCI</td><td>0</td><td>1</td></tr><tr><td>*SPI</td><td>1</td><td>1</td></tr></table>	BOOT_DEVICE	GNT0	GNT1	LPC	0	0	PCI	0	1	*SPI	1	1		Inter Pu Hi  SPI
BOOT_DEVICE	GNT0	GNT1													
LPC	0	0													
PCI	0	1													
*SPI	1	1													
PGNT-2	(inter pu)	*(-O),Desktop not pull low	DMI AC Coupling Low: Full Voltage Mode	TestPoint											
HDA_SDO	*POWERED BY EPW(-O)	POWERED BY CORE(inter pu)	NAND VCCQ PWR WELL SEL												
HDA_SYNC	*1.5V(-O)	1.8V	OD PLL VR SUPPLY SEL												
SPI_MOSI	*EN(-O)	DIS(inter pu)	TPM FUNCTIONALITY TPM DISABLED WHEN SAMPLED LOW												
NVR_ALE	*(10K)		DANBURY Technology Enable Enable When Sampled High												
NVR_CLE	*(-O)		DMI Termination Voltage DC Coup: TX/RX To VCC Is Sampled High												
INIT3_3V_N		*(-O)	Configurable CPU Output, Stronger If Low												
SPKR	*EN(1K)	DIS	STUFF TO ENABLE NO-REBOOT OPTION AT POWER-UP (CONFIGURATION STRAPPING).												
PCH_INTVRMEN	*EN(390K)		ENABLE INTERGRATED 1.05V SUS VRM.												
PCH_PU_GP33															
IGC_EN_N		*EN	INTEGRATED CLOCK CHIP ENABLE, Stuff Low For Full Clock Integration Enable.												
VCCVRM_EN	*EN(inter pu)	DIS(-O)	OD PLL VR(VccCLK,Vccap11EXP, VccFDIPLL,VccSATAPLL; DG P383)												
PCH_GP15	*EN(10K)	DIS	INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) WITH CONFIDENTIALITY												

PCI ROUTING

PCI1	AD17	INTA,B,C,D	PREQ-1	PGNT-0
------	------	------------	--------	--------

FAN_TAC1	CPU_FAN
FAN_CTL1	CPU_FAN
TMPIN1	SYS_Temp
VIN0	VCORE
VIN1	V_DIMM